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Interfacing ISP1161x to NEC V832 Processor

January 2003

Application Note

Rev. 2.2

Revision History:

Rev.	Date	Descriptions	Author
2.2	Jan 2003	• Updated the schematic section. • Updated Figure 4-1. • Removed the section on suspend and resume	Jason Ong
2.1	Sep 2002	• Updated to the latest Philips document template • Changed ISP1161x to ISP1161x • Changed the file name from INTFG_1161_TO_NECV832-02.pdf.	Kunzang Dolma
2.0	Oct, 2001	Updated schematic to reflect use of ES2	Jason Ong
1.0	Aug 2001	First release	Socol Constantin

Note: ISP1161x denotes any Philips USB single-chip host and device controller whose name starts with 'ISP1161', this includes ISP1161A, ISP1161A1 and any future derivatives.

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Note: ISP1161x denotes any Philips USB single-chip host and device controller whose name starts with 'ISP1161', this includes ISP1161A, ISP1161A1 and any future derivatives.

1. Overview

The unique design of Philips ISP1161x allows it to be used both as a Host Controller (with two downstream facing ports), and a Device Controller (with one upstream facing port). These ports may be independently accessed, enabling simultaneous connection as a Host Controller and a Device Controller.

When ISP116x is integrated into a personal digital assistant (PDA) or handheld personal computer (HPC), it is usually connected to the external bus interface of a Reduced Instruction Set Computer (RISC) processor. This application note deals with the critical issues in the ISP116x's embedded design, using the NEC V832 RISC processor as a concrete example.

2. ISP1161x Interface Signals to a RISC Processor Bus

ISP1161x's processor bus interface is designed for a simple direct connection with a RISC processor. The data transfer can be done in the Programmed I/O (PIO) or direct memory access (DMA) mode. The estimated maximum data transfer rate on ISP1161x's generic processor bus is approximately 15 Mbyte/s. This is based on an ISP1161x internal clock frequency value of 48 MHz. To achieve the maximum data transfer rate on the host processor bus, ISP1161x contains a ping pong structured RAM that allows alternative access from the RISC processor or from the internal Host Controller and the Device Controller. The ping pong memory is separately allocated for the Host Controller and the Device Controller. The Host Controller uses 2 kbytes of the ping memory and 2 kbytes of the pong memory in its allocated memory. The Device Controller uses 1.5 kbytes for each of the ping and the pong memory in its own memory.

The main ISP1161x signals to consider for connecting to the NEC V832 RISC processor are:

- A 16-bit data bus: (D[15:0]) for ISP1161x, which is "little endian" compatible.
- Two address lines (A0 and A1) necessary for complete addressing of the ISP1161x internal registers:
  - **A0 = 0 and A1 = 0**—Selects the Data Port of the Host Controller
  - **A0 = 1 and A1 = 0**—Selects the Command Port of the Host Controller
  - **A0 = 0 and A1 = 1**—Selects the Data Port of the Device Controller
  - **A0 = 1 and A1 = 1**—Selects the Command Port of the Device Controller.
- One $\overline{\text{CS}}$ line used to select ISP1161x in a certain address range of the host system. This input signal is active LOW.
- $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are common read and write signals. These signals are active LOW.
- Two DMA channel standard control lines: DREQ1, DREQ2, DACK1, DACK2 and EOT (one channel is used by the Host Controller and the other channel is used by the Device Controller). These signals have programmable active levels.
- Two interrupt lines:
  - INT1 (used by the Host Controller), and
  - INT2 (used by the Device Controller).

  Both have programmable level or edge, and polarity (active HIGH or LOW).
- The CLKOUT signal has a default power-on frequency of 12 MHz and the maximum value of 48 MHz.
- The $\overline{\text{RESET}}$ signal is active LOW.

3. NEC V832 (uPD705102)

This section highlights the main features of the NEC V832 processor of special interest for connecting to ISP1161x.

The NEC V832 processor divides its memory space into eight blocks, each having the following features that depend on the internal configuration settings:

- Bus size: 16 or 32 bits can be independently set for each area.
- Number of wait cycles can be independently set for each area. The total number of additional wait states inserted is equal to the biggest number of wait-states required by the READY signal or specified by the wait-state control bits (0 to 7 wait-states for blocks 1 through 4, and 7or 0 to 15 wait-states for blocks 5 and 6).
- Setting the type of space for each area will enable a direct connection to several possible types of memory: SRAM or ROM (blocks 1 through 7), SDRAM (block 0 and 1) and I/O (blocks 3 through 6).
- For correct data alignment, matching data width with endian is necessary. The ISP1161x connection will require a 16-bit/ little endian configuration of the selected memory area. The data bus width can be selected by setting the BWn (where n can take any value from 1 to 6) bit in the DBC register of NEC V832, and little endian corresponds to normal operation mode of V832.

ISP1161x can be connected as I/O (using IOWR#, IORD#, nBEN# and CSn#, where n can take any value from 3 to 6) or SRAM (using MWR#, MRD#, nBEN#, CSn#, where n can take any value from 1 to 6).

4. Considerations in Timing Diagrams and WAIT States

This section presents a short study of the timing diagrams of the main bus cycles of both ISP1161x and NEC V832.

According to the ISP1161x datasheet specifications, a read cycle requires the following main timing parameters (the requirements of the write cycle are similar):

- t_{RL} = 33 ns ($\overline{RD}$ LOW pulse width—minimal value required by ISP1161x),
- t_{RHRL} = 110 ns ($\overline{RD}$ HIGH to next $\overline{RD}$ LOW—minimal value required by ISP1161x) and
- t_{RHDZ} = 3 ns ($\overline{RD}$ hold time, minimal value that can be expected from ISP1161x).
- t_{RC} = 143 ns (will result as a sum of t_{RL} and t_{RHRL})
- t_{SHSL} = 300 ns (first $\overline{RD}$/$\overline{WR}$ after command).

For a detailed analysis of a timing diagram, consider the access of an ISP1161x internal register (for example, the Control Register of the Host Controller). It requires two phases: writing the address (index) of the selected register into the Command Port; then only data transfer access (RD/WR) may take place.

The timing diagram in Figure 4-1 describes the two phases of accessing the ISP1161x:

- The first phase is accessing the Command (control) Port of ISP1161x, to write the address (index) of the data port that will be accessed. In this phase $\overline{CS}$ is active, the data lines D[15:0] contain the desired address. The $\overline{WR}$ pulse will be activated and will latch the data. Note the value of t_{SHSL} that represents the minimum time required between occurrence of the first phase and the second phase. As an example of the Host Controller "Control Register" a value of 01H will be transferred during a $\overline{RD}$ operation and 81H during a $\overline{WR}$ operation.
- The second phase consists of the access (read or write) to the data port selected by the address latched in the previous phase. Two timing diagrams are combined again in this second phase: one for the read access and one for the write access. A series of $\overline{RD}$ and $\overline{WR}$ pulses are shown in the diagram to define the timing requirements between two consecutive accesses to ISP1161x: t_{RHRL}, t_{WHWL}, t_{RC}, t_{WC}, t_{RLDV}, as specified in the datasheet.

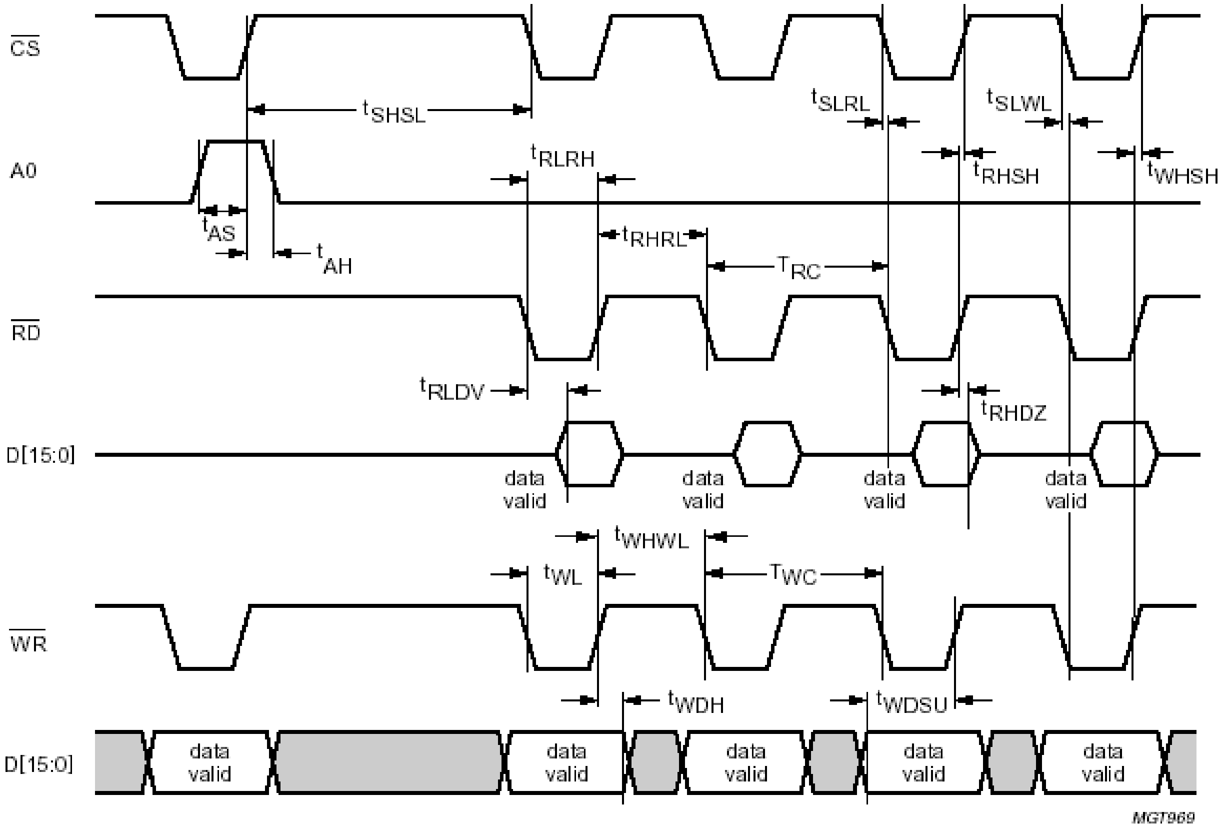


Figure 4-1: Programmed Interface Timing (16-bit Read/Write)

When the ISP1161x connection area is defined as SRAM, ISP1161x will operate correctly for a bus clock CKIO = 33 MHz. Timing measurements show that inserting wait-states in the standard bus cycles of the NEC V832 is unnecessary. Nevertheless, we will describe wait-state insertion, to cater for cases when faster bus cycles are used for accessing ISP1161x.

Wait states can be inserted using hardware or software. Both solutions will delay the rising edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to the next CKIO cycle and will determine an elongation of the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ LOW pulse that can be calculated as:

t_W = W x T(CKIO); where: (W) is the number of wait states desired.

T(CKIO) is the cycle length of CKIO.

Note: the value of t_{RHRL} will not be modified by the number of wait states inserted by any of the solutions mentioned earlier. The value of this parameter must be calculated and correctly adjusted according to the number and length of instructions executed by the NEC V832 processor between two successive accesses to ISP1161x. The "software solution" for wait-state insertion in a bus cycle is simple and is preferred in a minimal configuration, if additional wait states are necessary.

5. Using interrupts

ISP1161x generates two interrupts on the INT1 and the INT2 pins, allocated for the Host Controller and the Device Controller, respectively. These interrupts occur depending on the setting of the interrupt registers.

Both INT1 and INT2 of the ISP1161x are programmable as active on level or edge and HIGH or LOW, as specified in the *HcHardwareConfiguration Register* and *DcHardwareConfiguration Register* of the Host Controller and Device Controller, respectively.

6. DMA Operation

ISP1161x's internal structure contains two DMA handlers: the Host Controller uses one, and the Device Controller uses the other. ISP1161x's DMA handlers can work in the DACK mode or in the 8237 mode by using the EOT (End Of Transfer) signal, according to the bits setting of the *Hardware Control* registers. Programming *HcDMAConfiguration*, *DcDMAConfiguration, HcTransferCounter* and the *DcDMACounter Registers* is necessary for defining the parameters of the DMA operation (transfer counter enable, DMA enable, burst length), separately for each of the Host Controller and the Device Controller. Details on programming of DMA registers can be found in the ISP1161x datasheet and the *ISP1161x Embedded Programming Guide*.

The connection of DMA channel signals from ISP1161x to the V832 can be achieved by connecting the DREQ1, DREQ2, DACK1 and DACK2 signals of ISP1161x to the DMARQ0, DMARQ1, DMAAK0, and DMAAK1 signals of V832, respectively, because of the flexible interfaces of both ISP1161x and the NEC processor. In this configuration, connect the ISP1161x's EOT signal to NEC V832's TC# input pin.

As shown in the following timing diagram, by asserting the DACK1 signal, the host system will allow data transfer to take place, allocating the bus for the ISP1161x. Both the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ data transfer cycles are contained in the timing diagram. The $\overline{\text{CS}}$ signal is not used by ISP1161x's internal selection logic, and the DMAAK1 and DMAAK2 signals will be used to define the bus owner that issued DREQ and is currently involved in the data transfer. No other system resource on the same bus will be accessed as long as the DMA cycle is in progress and occupies the bus. The series of DMAAK1 or DMAAK2 active pulses determine the time allocated to the DMA data transfer.

You can simultaneously use both the DMA channels of the ISP1161x Host Controller and the Device Controller; by setting the DMA priority bits of V832, to define the DMA channel that will first participate in the data transfer.

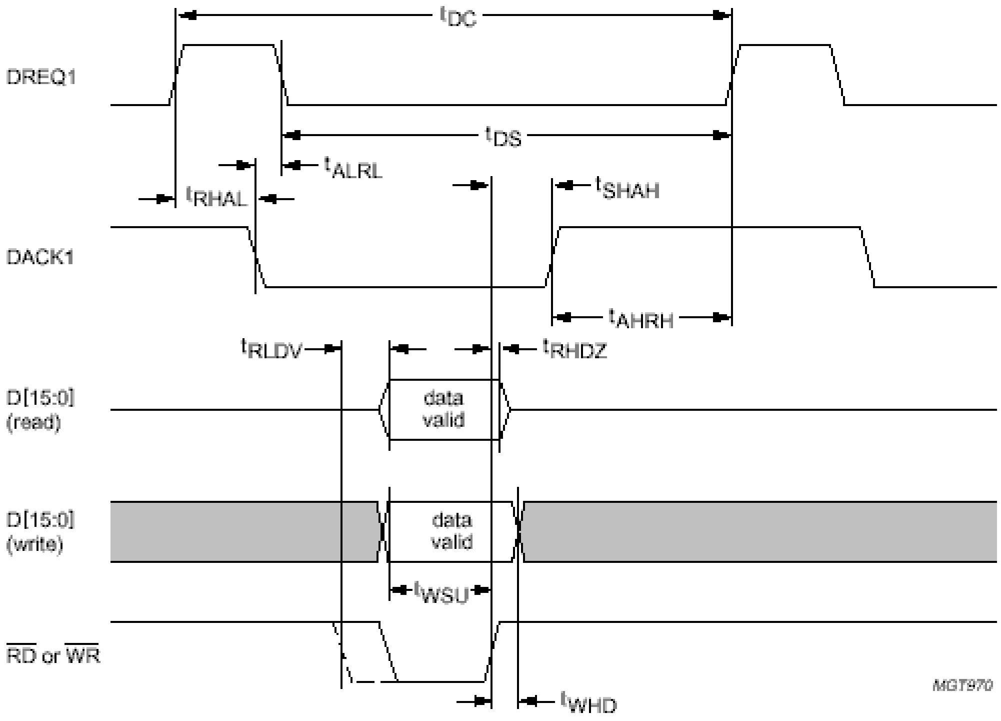


Figure 6-1: Host Controller Single-Cycle DMA Timing

A DMA burst access of up to 8 cycles for the ISP1161x host DMA handler and up to 8 cycles for the device DMA handler can be defined in the *HcDMAConfiguration* and *DcDMAConfiguration Registers*.

If necessary, add wait states to the basic DMA cycle to create longer $\overline{\text{RD}}$/$\overline{\text{WR}}$ and DMAAK pulses. To learn how to insert wait states, see Section 4.

7. Schematic Diagram

The following schematic diagram shows ISP1161x connected to the NEC V832 processor, in a minimal hardware configuration.

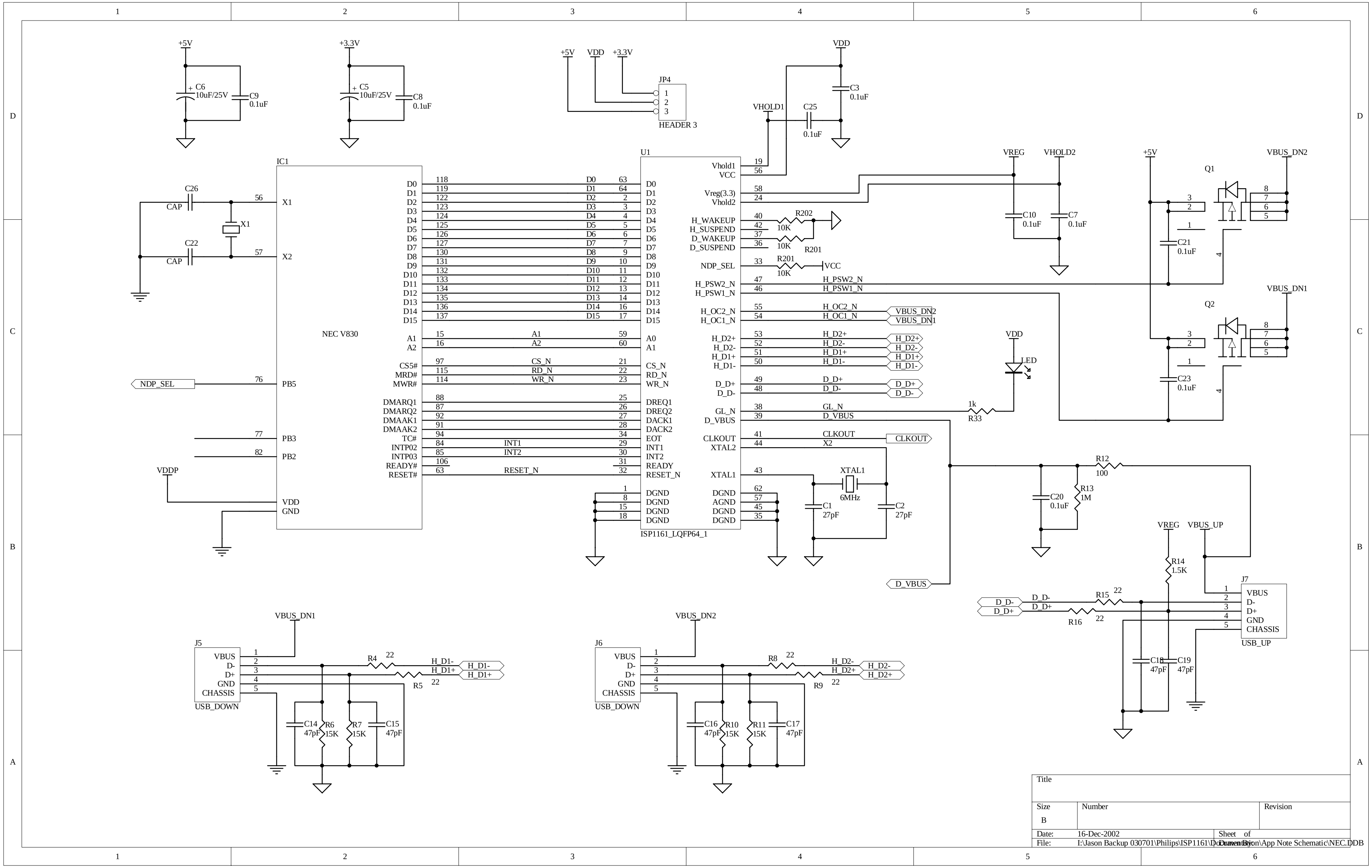
In this example schematic, the ISP1161x is simply selected by CS5# (in a more complex configuration some glue logic may be required to generate a CS signal composed of CSn and several address lines).

Input signals $\overline{\mathrm{H\_OC1}}$ and $\overline{\mathrm{H\_OC2}}$ are used by the ISP1161x to detect an overcurrent on the downstream facing ports. Since separate overcurrent detection and protection circuits are implemented for each ISP1161x downstream facing port in the, detection of an overcurrent on a downstream facing port will have power turned off at that port only. Connecting the voltages of the two downstream ports VBUS_DN1 and VBUS_DN2 to the $\overline{\mathrm{H\_OC1}}$ and $\overline{\mathrm{H\_OC2}}$ pins enables detection of the current value by sensing the voltage drop on Q1 and Q2 that are PMOS transistors with very low switch-on resistance Rds(on). Selection between Q1 and Q2 depends on the desired maximum current value and this determines the value of Rds(on). For example, if the allowed maximum current is approximately 0.5 A, a voltage drop of 75 mV will trigger the overcurrent circuitry and Rds(on) of approximately 150 MΩ will result. Connecting the ISP1161x input pins $\overline{\mathrm{H\_OC1}}$ and $\overline{\mathrm{H\_OC2}}$ to +5 V will disable ISP1161x's internal overcurrent protection. An external overcurrent protection circuit may also be used.

Detection of a connection on the upstream port is achieved by connecting VBUS_UP to pin D_VBUS of ISP1161x. It is recommended, if possible, to implement a hybrid power solution, by using VBUS_UP to provide power to ISP1161x and an external power source for the rest of the system.

The GoodLink™ ($\overline{\mathrm{GL}}$) output signal indicates (using an LED) the status of the USB device and helps in troubleshooting the USB connection.

The $\overline{\mathrm{RESET}}$ input signal of the ISP1161x is connected to the system RESET signal.



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File: I:\Jason Backup 030701\Philips\ISP1161\Documentation\App Note Schematic\NEC.DDB

8. References

- *Universal Serial Bus Specification Rev. 2.0*
- *ISP1161A1 Full-speed Universal Serial Bus single-chip host and device controller* datasheet
- *ISP1161A Full-speed Universal Serial Bus single-chip host and device controller* datasheet
- *ISP1161 Full-speed Universal Serial Bus single-chip host and device controller* datasheet
- *Interfacing ISP1161x to Hitachi SH7709 RISC Processor* application note
- *ISP1161x Embedded Programming Guide.*

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